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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,785	02/20/2004	Thomas Richardson	03-2049 / LSI.94US01	6953

84654 7590 11/12/2009

COCHRAN FREUND & YOUNG LLC
LSI CORPORATION
2026 CARIBOU DRIVE
SUITE 201
FORT COLLINS, CO 80525

EXAMINER	
HASSAN, AURANGZEB	
ART UNIT	**PAPER NUMBER**
2182	

MAIL DATE	DELIVERY MODE
11/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,785	RICHARDSON ET AL.	
	Examiner	Art Unit	
	AURANGZEB HASSAN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 12 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya (US Patent Number 5,809,330) in view of Nakashima (US Patent Number 6,029,211).

3. As per claim 12, Ninomiya teaches a method for determining the function of a circuit board (expansion unit, element 2, figure 1) disposed in a slot (detection via connectors, element 26 and 27, figure 1) in an enclosure comprising the steps of:

displaying an identifying characteristic of the slot inside of the enclosure (expansion connector detecting various possible characteristics in the form of multitude of expansion devices, column 7, lines 53 – 58, displaying the identifying characteristic as per the specification 0020 is represented by an obstruction of the light by the circuit board which is analogous to the obstruction of the photo-sensors as seen in column 8, lines 4 - 20, and identification is also capable through detection of a change in voltage to certain pins of the connector, column 8, lines 31 – 34, the identifying characteristic in itself is a sensor that can determine a change in its state);

detecting the circuit board (upon connection routed to system bus for characteristics further determined by photo-sensors, column 7, lines 66-67, column 8, lines 1 – 10, the photo-sensors are the initiator in the process to determine the characteristic of the inserted option card, see further explanation for claim 1); and

directing the circuit board to perform the function associated of the slot (CPU enables connectors and determining of characteristics between expansion unit and main unit, element 11, figure 1).

Ninomiya does not teach a characteristic of a binary representation that allows for a multifunction circuit that associates the particular function based on the detected binary characteristic.

Nakashima teaches a method in which a characteristic is identified in a binary representation for directing a multifunction circuit board to perform a particular function associated with the detected characteristic (column 6, lines 40 – 58, CIS characteristic utilized to determine function of card) detecting the displayed characteristic on the circuit board (column 6, lines 31 – 39); interpreting the detected characteristic on the circuit board (column 6, lines 34 – 39, function); and directing the circuit board to perform the function associated with the interpreted characteristic of the slot (column 6, lines 40 – 43).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Ninomiya with that of Nakashima. One of ordinary skill would make such modification in order to reduce overhead of driver installation of functions not being utilized by the PC (column 2, lines 18 - 24).

4. As per claim 13, Ninomiya teaches a method wherein said means located within said enclosure for displaying a characteristic of the slot comprises means for generating at least one signal, and at least one tab disposed within the interior of the slot capable of substantially reducing the at least one signal (light from photo emitter to photoreceptor is considered at least one signal generated, column 8, lines 7 – 10).

5. As per claim 14, Ninomiya teaches a method wherein said means disposed on said circuit board for detecting the characteristic of the slot comprises means for detecting the at least one signal (photo sensors, elements 30-31, figure 1).

6. As per claim 15, Ninomiya teaches a method wherein said means for generating at least one signal comprises a source of light (photo emitter, column 8, lines 7 – 10), and wherein said means for detecting the characteristic of the slot comprises at least one light detector (photo-sensor, element 30, figure 1) adapted for detecting light generated from said source of light.

7. As per claim 16, Ninomiya teaches a method wherein said means displaying a characteristic of the slot comprises at least one source of light; and said means for detecting the characteristic of said slot comprises at least one light detector adapted for detecting light generated by said at least one source of light, whereby the pattern characteristic of the slot is reproduced by said at least one light detector.

8. As per claim 17 a method wherein said means for detecting the characteristic of the slot comprises at least one microswitch (microswitch, column 8, lines 33 – 35) and said means for displaying a characteristic of the slot comprises at least one projection positioned on a wall of said enclosure disposed in a pattern characteristic of the slot and adapted to actuate one of said at least one microswitch when said circuit board is inserted into the slot, such that the characteristic of the slot is sensed by said at least one microswitch (mechanically detected by means of microswitch through detection of a change in voltage to certain pins of the expansion connector, column 8, lines 27 - 35).

9. Claims 1 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya in view of Nakashima further in view of Lee (US Patent Number 5,748,912).

10. As per claim 1, Ninomiya teaches an apparatus for determining the function of a circuit board (expansion unit, element 2, figure 1) disposed in a slot (detection via connectors, element 26 and 27, figure 1) in an enclosure and in electrical communication with said enclosure (laptop-type environment, figure 1), which comprises in combination: (a) means located within said enclosure for displaying an identifying characteristic of the slot (expansion connector detecting various possible characteristics in the form of multitude of expansion devices, column 7, lines 53 – 58); (b) means disposed on said circuit board for detecting the characteristic (upon

connection routed to system bus for characteristics further determined by photo-sensors, column 7, lines 66-67, column 8, lines 1 – 10, the photo-sensors are the initiator in the process to determine the characteristic of the inserted option card); and (c) a processor for interpreting the detected characteristic and for directing said circuit board to perform the function associated therewith (CPU enables connectors and determining of characteristics between expansion unit and main unit, element 11, figure 1).

Ninomiya does not teach a characteristic of a binary representation that allows for a multifunction circuit that associates the particular function based on the detected binary characteristic.

Nakashima teaches a method in which a characteristic is identified in a binary representation for directing a multifunction circuit board to perform a particular function associated with the detected characteristic (column 6, lines 40 – 58, CIS characteristic utilized to determine function of card).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Ninomiya with that of Nakashima. One of ordinary skill would make such modification in order to reduce overhead of driver installation of functions not being utilized by the PC (column 2, lines 18 - 24).

Ninomiya/Nakashima does not disclose a processor disposed on said circuit board.

Lee analogously teaches an option card (figure 2b) with a processor disposed on said circuit board (CPU 402, figure 4a).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to insert the option card of Lee into the option card slot of Ninomiya/Nakashima. One of ordinary skill in the art would be motivate to make such modifications in order to allow for an efficient and flexible means for users to replace a processor in a unit without exorbitant costs (column 2, lines 1 – 10).

11. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claim 2, Ninomiya teaches the apparatus wherein said means located within said enclosure for displaying a characteristic of the slot comprises means for generating at least one signal, and at least one tab disposed within the interior of the slot capable of substantially reducing the at least one signal (light from photo emitter to photoreceptor is considered at least one signal generated, column 8, lines 7 – 10).

12. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claim 3, Ninomiya teaches an apparatus wherein said means disposed on said circuit board for detecting the characteristic of the slot comprises means for detecting the at least one signal (photo sensors, elements 30-31, figure 1).

13. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claim 4, Ninomiya teaches an apparatus wherein said means for generating at least one signal comprises a source of light (photo emitter, column 8, lines 7 – 10), and wherein said means for detecting the characteristic of the slot comprises at

least one light detector (photo-sensor, element 30, figure 1) adapted for detecting light generated from said source of light.

14. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claim 5, Ninomiya teaches an apparatus wherein said at least one tab is disposed in a pattern characteristic of the slot, and said at least one light detector, reproduces the pattern characteristic of the slot (indication of the option card generated based on signal DTE2, column 8, lines 21 – 27).

15. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claim 6, Ninomiya teaches an apparatus wherein the light generated from said source of light is substantially reduced by said at least one tab when said at least one tab is disposed between said source of light and said at least one light detector (passage of light block upon insertion of option card substantially reducing the light generated from the source in reference to the opposing photo-sensor, column 8, lines 21 – 24).

16. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claims 7 and 9, Ninomiya teaches an apparatus wherein said at least one source of light comprises at least one light emitting diode (photo-emitter, column 8, lines 7 – 10) and said at least one light detector comprises a charge-coupled detector (photo-receptor, column 8, lines 10 – 13).

17. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claim 8, Ninomiya teaches an apparatus wherein said means displaying a characteristic of the slot comprises at least one source of light; and said means for detecting the characteristic of said slot comprises at least one light detector adapted for detecting light generated by said at least one source of light, whereby the pattern characteristic of the slot is reproduced by said at least one light detector.

18. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claim 10 an apparatus wherein said means for detecting the characteristic of the slot comprises at least one microswitch (microswitch, column 8, lines 33 – 35) in electrical communication with said processor, and said means for displaying a characteristic of the slot comprises at least one projection positioned on a wall of said enclosure disposed in a pattern characteristic of the slot and adapted to actuate one of said at least one microswitch when said circuit board is inserted into the slot, such that the characteristic of the slot is sensed by said at least one microswitch (mechanically detected by means of microswitch through detection of a change in voltage to certain pins of the expansion connector, column 8, lines 27 - 35).

19. Claims 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya in view of Nakashima further in view of Lee further in view of Pope et al. (US Patent Number 4,781,066).

20. Ninomiya/Nakashima modified by the teachings of Lee as applied in claim 1 above as per claims 11 and 18, fails to teach and apparatus wherein said means disposed on said circuit board for detecting the characteristic of the slot comprises a Hall-effect apparatus.

Pope et al. analogously teaches an apparatus wherein said means disposed on said circuit board for detecting the characteristic of the slot comprises a Hall-effect apparatus (element 75, figure 6, column 6, lines 36 – 40).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Ninomiya and Lee with the above teaches of Pope et al. One of ordinary skill would have been motivated to make such modification in order to have a detection system that permits enhanced sensitivity and noise immunity in the system (column 7, lines 7 – 10).

Response to Arguments

21. Applicant's arguments filed 7/29/2009 have been fully considered but they are not persuasive. The applicant argues that the step of displaying an identifying characteristic of the slot, the step of detecting the binary representation of the displayed characteristic on the multifunction circuit board and the step of interpreting the binary representation of the detected characteristic are not taught by the prior art.

22. With regards to the applicants arguments the Examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Examiner relies upon Ninomiya for the teachings of displaying an identifying characteristic and the functionality therein. Ninomiya utilizes the characteristic in order to allow for function of the card inserted in the slot. Nakashima is relied upon for the binary representation which can be utilized in characterizing an identifying mechanism as seen in column 6, lines 40 - 67. The Examiner notes that in the prosecution the Examiner has advised in response to the Applicant's arguments that the binary representation of tabs within the slot are not clearly recited in the independent claims (Final Rejection arguments 10/7/2008). Currently claims 5 and 6 are the closest in terms of actually claiming what was argued in the application history however the claims still do not clearly necessitate that there are tabs within the slot that are arranged in a binary pattern which can control functionality of the slot and overall system by a comparison of the amount of light “substantially reduced” by the particular pattern of tabs. In order to enhance compact prosecution the Examiner suggests amendments to the independent claims which include the teachings of claim 6 with the clarification that the pattern characteristic of the slot is a binary pattern formed by the functionality of the tabs as can be seen by figure 1 of the instant application. Amendments therein would overcome the art of record and would best provide for furthering of prosecution.

Applicant is encouraged to contact the Examiner for further clarification of the proposed concepts which best exemplify the invention as interpreted by the Examiner.

Conclusion

23. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AURANGZEB HASSAN whose telephone number is (571)272-8625. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on 571-272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182